WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a logic circuit including a logic transistor formed of an insulated gate type field effect transistor as a component thereof and executing a prescribed processing; and

memory circuitry for storing at least data to be used by said logic circuit, said memory circuit including a first circuit receiving a first voltage for operation and a second circuit receiving a second voltage higher than said first voltage for operation,

said first circuit including as a component thereof a first-type insulated gate field effect transistor having a gate insulating film same at least in thickness as said logic transistor, said second circuit including as a component thereof a second-type insulated gate field effect transistor having a gate insulating film thicker than a gate insulation film of said logic transistor.

2. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry further includes a memory cell array having a plurality of memory cells arranged in rows and columns, and

said first circuit includes column-related peripheral circuitry for performing an operation related to a column selection in said memory cell array.

3. The semiconductor integrated circuit device according to claim 1, wherein

said first-type insulated gate field effect transistor is an insulated gate field effect transistor formed in a same manufacturing step as said logic transistor.

4. The semiconductor integrated circuit device according to claim 1, wherein

said first circuit includes a peripheral control circuit for generating an operation control signal for controlling an internal operation according to a control signal from said logic circuit.

5. The semiconductor integrated circuit device according to claim 2, wherein

said column-related peripheral circuitry includes a column selecting circuit for selecting a column in said memory cell array and a writing/reading circuit for writing and reading data to and from a column selected by said column selecting circuit.

6. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry further includes:

a memory cell array having a plurality of memory cells arranged in rows and columns, the memory cell including said second-type insulated gate field effect transistor as a component thereof;

a plurality of word lines arranged corresponding to respective rows of the memory cells, each of the word lines being connected to a corresponding row of the memory cells; and

a plurality of bit line pairs arranged corresponding to respective columns of the memory cells, each of the bit line pairs being connected to a corresponding column of the memory cells,

said second circuit includes:

a row selecting circuit for driving a word line provided corresponding to an addressed row into a selected state; and

a bit line equalize circuit for equalizing potentials of the plurality of bit line pairs in a stand-by cycle.

7. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry further includes an internal voltage generating circuit including said second-type insulated gate field effect transistor as a

component thereof, for generating an internal voltage at a predetermined level.

8. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry further includes:

a memory cell array having a plurality of memory cells arranged in rows and columns; and

a plurality of sense amplifier circuits provided corresponding to the columns of the memory cells, each for sensing and amplifying data on a memory cell on a corresponding column,

the sense amplifier circuit including said first-type insulated gate field effect transistor as a component thereof.

9. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry further includes:

a plurality of memory blocks each having a plurality of memory cells arranged in rows and columns and a plurality of bit line pairs provided corresponding to the columns of memory cells and connected to corresponding columns of the memory cells, said plurality of memory blocks being arranged in direction of the columns; and

a plurality of sense amplifier circuits provided corresponding to the bit line pairs of the memory blocks so as to be shared between memory blocks adjacent in the direction of the columns, for differentially amplifying potentials of corresponding bit line pairs when made active, said plurality of sense amplifier circuits each including said first-type insulated gate field effect transistor as a component thereof; and

a plurality of bit line isolation gates each provided between each bit line pair and a corresponding sense amplifier circuit for isolating said bit line pair and said corresponding sense amplifier circuit in an acceleration test mode, the bit line isolation gate including said second-type insulated gate field effect transistor.

10. The semiconductor integrated circuit device according to claim 9, further comprising:

a plurality of bit line equalize circuits provided corresponding to the bit line pairs, for transmitting a bit line equalize voltage to corresponding bit line pairs when made active; and

a test control circuit for activating the bit line equalize circuits and raising said bit line equalize voltage in said acceleration test mode, the bit line equalize circuit including said second-type insulated gate field effect transistor as a component thereof, the bit line equalize circuit being isolated from a corresponding sense amplifier circuit by the bit line isolation gate in said acceleration test mode.

11. The semiconductor integrated circuit device according to claim 8, wherein

said memory circuitry further includes:

a sense power supply line; and

a plurality of sense drive transistors each provided for a prescribed number of the sense amplifier circuits and each formed of said second-type insulated gate field effect transistor for connecting the sense amplifier circuits and the sense power supply line when made conductive.

12. The semiconductor integrated circuit device according to claim 8, wherein

said memory circuitry further includes:

a sense power supply line; and

a plurality of sense amplifier drive transistors each provided for a prescribed number of the sense amplifier circuits and each formed of said first-type insulated gate field effect transistor for connecting said sense power supply line to the sense amplifier circuits, back gates of said plurality of sense amplifier drive transistors receiving a voltage larger in absolute value than a voltage on said sense power supply line.

13. The semiconductor integrated circuit device according to claim

12, wherein

said memory cell array is divided into a plurality of memory blocks along directions of the rows and the columns, and

the sense amplifier drive transistor is provided in a region between memory blocks adjacent in the direction of the rows.

14. The semiconductor integrated circuit device according to claim 11, wherein

said memory cell array is divided into a plurality of memory blocks along directions of the rows and the columns, and

the sense amplifier circuit is provided in a region between memory blocks adjacent in the direction of the columns, and

the sense amplifier drive transistor is provided in a crossing region of a region for arranging the sense amplifier circuit and a region between memory blocks adjacent in the direction of the rows.

15. The semiconductor integrated circuit device according to claim 1, wherein

said memory circuitry includes:

a plurality of memory blocks each including a plurality of memory cells arranged in rows and columns and a plurality of bit line pairs provided corresponding to respective columns and each connected to a corresponding column of the memory cells, and provided in alignment in directions of the rows and columns, said plurality of memory blocks being formed in a plurality of first substrate regions of a first conductivity type isolated from each other, each said first substrate region being formed surrounded by a second substrate region of a second conductivity type, said second substrate region being isolated by a third substrate region of said first conductivity type in a region between memory blocks adjacent in a direction of the columns;

an equalizing insulated gate field effect transistor provided corresponding to each of the columns of the memory cells and formed in said first substrate region, for equalizing voltages on bit lines in a

corresponding column;

a bit line isolation insulated gate field effect transistor formed corresponding to each column of the memory cells in said first substrate region between a region for forming said equalizing insulated gate field effect transistor and said third substrate region;

a plurality of sense amplifier circuits provided corresponding to the columns of the memory cells for differentially amplifying potentials on bit lines in corresponding columns when made active, each said sense amplifier circuit including a first sense amplifier transistor formed in a fourth substrate region of the second conductivity type provided to extend in a direction of rows so as to divide said third substrate region in the direction of the columns into first and second divisional regions, and a second sense amplifier transistor formed in said first divisional region; and

a column selecting gate insulated gate field effect transistor provided in said second divisional region and corresponding to each said sense amplifier circuit for connecting a corresponding sense amplifier circuit to an internal data line in response to a column selecting signal,

the sense amplifier circuits are shared between memory blocks adjacent in the direction of the columns,

said column selecting gate insulated gate field effect transistor and the first and second sense amplifier transistors have a gate insulating film same in thickness as said logic transistor, and

said bit line equalizing transistor and said bit line isolation insulated gate field effect transistor have a gate insulating film greater in thickness than said logic transistor.

16. The semiconductor integrated circuit according to claim 15, wherein

said memory circuitry further includes:

a first sense amplifier drive transistor formed in the second substrate region between memory blocks adjacent in the direction of the rows, for transmitting a first power supply voltage to the sense amplifier circuits provided corresponding to said memory blocks adjacent in the direction of

the rows when made conductive; and

a second sense amplifier drive transistor formed in said first substrate region of at least one of said memory blocks adjacent in the direction of the rows for transmitting a second power supply voltage to said sense amplifier circuits when made conductive, the first and second sense amplifier drive transistors being the first-type insulated gate field effect transistors.

17. The semiconductor integrated circuit device according to claim 15, wherein

said memory circuitry further includes:

a first sense amplifier drive transistor formed in said third substrate region in a crossing region of a region between memory blocks adjacent in the direction of the rows and a region for providing the sense amplifier circuits, for transmitting a first power supply voltage to corresponding sense amplifier circuits when made conductive; and

a second sense amplifier drive transistor formed in said first divisional region for transmitting a second power supply voltage to said corresponding sense amplifier circuits when made conductive, the first and second sense amplifier drive transistors being the second-type insulated gate field effect transistors.